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A wireless-feeding capacitive electrode mechanism for achieving massive nanosecond parallel-discharge EDM for large-size wafer flattening

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ABSTRACT

The single-crystal silicon carbide (SiC) wafer diameter is increasing beyond 8 in posing significant challenges to conventional mechanical wafer-processing methods. This study presents an innovative capacitive electrode method for electrical discharge flattening (EDF) of as-sliced large 4H-SiC wafers. The capacitive electrode can be divided into near-infinite units, which significantly reduces the working gap capacitance and enables the generation of a mass of parallel discharges with a nanosecond pulse duration (< 200 ns). This approach offers significant advantages in achieving high efficiency and surface finish simultaneously, regardless of the increase in wafer size. This novel electrode design allows wireless electricity feeding via electrostatic induction, which significantly facilitates the integration of parallel electrode units. Furthermore, a sinusoidal voltage is demonstrated for the first time to identify and promote a parallel discharge state. A model was devised to quantitatively describe the overall process. Using this model, the relationship between the gap voltage, discharge energy, and capacitive electrode properties was predicted, revealing a parallel discharge mechanism. The capacitive electrode mechanism was validated via EDF experiments on a 4H-SiC wafer. Notably, >33 parallel discharges within 6 μs were achieved in a single pulse, resulting in a minimum discharge energy of 0.312 μJ (peak current: 0.18 A, duration: 160 ns) and a surface roughness of Ra 42 nm. Moreover, a machining speed of 0.5 μm/min was achieved on a 4 in wafer, representing an improvement of an order of magnitude compared to conventional non-parallel discharge methods.

1. Introduction

Owing to their superior physical properties, such as a wide bandgap, high thermal conductivity, high breakdown electric field, and high electron mobility, single-crystal silicon carbides (SiC) have become emerging key materials for next-generation electronic technology for high-power, high-voltage, and high-frequency applications [1]. SiC substrates are processed into wafers from single-crystal ingots through slicing, grinding, and lapping, followed by multistep mechanical polishing and chemical mechanical polishing (CMP) to remove the damaged layer of the wafer surface caused by the previous process and reduce the surface roughness. As the final step of wafer planarization, CMP produces an ultra-smooth surface finish below Ra 0.1 nm [2,3], with a very low material removal rate (typically <1 μm/h) [4–6]. Therefore, grinding/lapping are crucial for preliminarily flattening the sliced wafers and thinning them to a uniform thickness, thereby minimizing the workload of CMP.

However, the exceptionally high hardness and brittleness of SiC make it challenging to process using conventional mechanical wafer-fabrication techniques. Diamond grinding wheels, which are widely utilized in SiC wafer grinding and thinning processes [7,8], tend to clog or wear out rapidly [9], leading to surface scratches, unstable machining forces, and high tool-consumable costs [10,11]. Additionally, the brittleness of SiCs makes them susceptible to brittle fractures, particularly under unstable force loading conditions [12]. This imposes stringent requirements on the rigidity and precision of machine tools. These problems become increasingly challenging as SiC wafers continue to increase in diameter (beyond 8 in) and decrease in thickness [13].

To meet the future manufacturing demands of large SiC wafers, Guan and Zhao [14] presented a non-contact wafer-flattening method based on pure electrical discharge machining (EDM). The absence of mechanical forces during EDM allows a 1 in-diameter SiC wafer to be

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thinned down to 30 μm without fracturing. Further, a dual-wafer intergrinding method was developed to double the machining efficiency and reduce the discharge energy to the μJ level [15]. This resulted in a surface finish with an Ra of 80 nm, which is comparable to that obtained by mechanical lapping [16,17]. Compared to grinding/lapping, EDM has no macro machining force, which reduces the stiffness and precision requirements for the machine tool equipment. Further, EDM does not require diamond abrasive tools to process SiC. Thus, EDM is superior in reducing manufacturing costs. However, achieving ideal surface quality when processing large-size wafers using the electrical discharge method remains a significant challenge. This is because the gap stray capacitance increases significantly with an increase in the wafer size, causing a significantly enlarged discharge energy and, consequently, a poor surface [18]. Moreover, ensuring processing efficiency while minimizing discharge energy is crucial. In the wafer-flattening process, the discharge energy or power frequency cannot be increased to prevent abnormal discharge damage to the wafers [19,20]. Therefore, simultaneously achieving high efficiency and surface finish during wafer fabrication has been a longstanding objective.

Generally, the surface integrity of EDM is determined by a single-discharge energy, and a lower discharge energy leads to better surface quality. However, the energy stored in the gap stray capacitances formed between the wires and the electrode-workpiece/worktable pair is inevitably released into the gap during discharge, causing a considerably higher discharge energy than pre-defined [21,22]. This gap stray capacitance problem is exacerbated as the electrode area increases, making it difficult to minimize discharge energy during the machining of large wafers. Several measures have been explored to reduce the effects of stray capacitance. Egashira and Mizutani [23] utilized open circuit voltages lower than 30 V in relaxation micro-EDM to minimize stored stray energy and successfully fabricated a tungsten micro-pin of 1 μm in diameter. However, low voltages may pose challenges for discharge ignition, leading to lower material removal efficiency. Koyano et al. [24] employed high-resistivity electrodes to limit the discharge current flowing from stray capacitances in a relaxation micro-EDM. This strategy successfully reduced the discharge energy, achieving a bottom surface finish of Rz 30 nm when machining φ0.3 mm micro-holes in stainless steel using an Si electrode with a resistivity of 0.65 Ω·cm. From a different perspective, Kunieda et al. [25] proposed an electrostatic induction feeding method (EIFM) to mitigate the influence of stray capacitance and achieved a surface roughness of Rz 0.23 μm in micro-hole machining (φ130 μm). However, when Yang and Wang [26] applied EIFM to large-area finishing (78.5 cm^2), the best surface finish obtained was Ra 0.3 μm, which is nearly an order of magnitude larger compared to micro-EDM [25]. This demonstrates the significant negative impact of the working-gap capacitance on large-area EDM finishing.

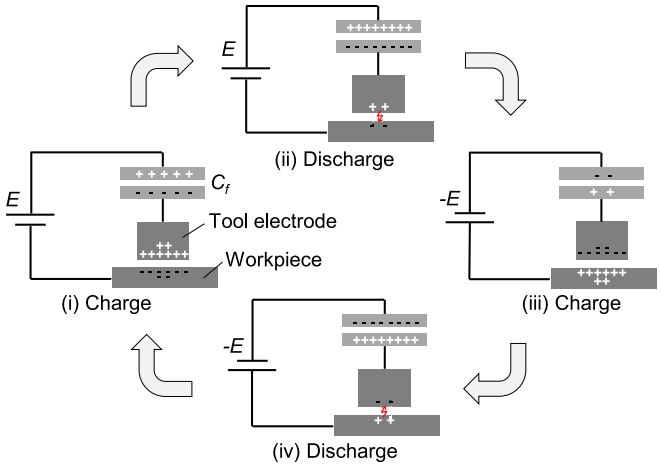


Fig. 1. Principle of the electrostatic induction feeding method (EIFM).

Mohri et al. [27] proposed dividing a large electrode into multiple partitions to reduce gap capacitance. Their results demonstrated that this divided electrode method effectively reduced the discharge energy, and a mirror-like surface finish with an Rmax of 0.5 μm was achieved on a large area of 100 cm^2.

However, as a machining technology, EDM generally exhibits low material removal rates (MRRs) because of the inherent nature of intermittent discharge generation. Only one discharge occurs at a specific location in a single pulse [18]. Therefore, achieving parallel discharges to increase the discharge frequency is an essential and indispensable approach for enhancing wafer processing efficiency, especially when attempting to simultaneously achieve both a high MRR and surface finish. In the multidivided electrode method developed by Mohri et al. [27], parallel discharges are achieved by connecting each divided electrode unit to a power supply through a series resistor. Based on the multidivided electrode method, Kunieda and Muto [28] employed a twin-electrode discharge system to create a multispark EDM with two parallel discharges, which achieved a 30 % enhancement in the removal rate and an 82 % enhancement in the energy efficiency when compared with traditional EDM methods. Han and Kunieda [29] developed a relaxation parallel EDM circuit that connected each divided electrode to a relaxation generator via a diode. The removal rate obtained with four electrodes was approximately 2.5 times faster than that obtained in conventional EDM under the same machining conditions of 50 A and 2 μs. Furthermore, Zhao et al. [30] developed a multi-discharge method based on the EIFM, which connects each divided electrode to a pulse generator through a feeding capacitance.

The EIFM improves process stability and reduces discharge concentration because the discharge interval can be controlled [31]. Yang et al. [32] applied this method for micro-hole array machining, demonstrating an almost fourfold enhancement in processing efficiency by utilizing six parallel copper rods with a diameter of φ2 mm in contrast to a single electrode. For the multidivided electrode method, increasing the number of divided electrodes and reducing the size of the electrode units allows for more parallel discharges or a smaller gap capacitance, significantly improving the processing efficiency and finishing accuracy. However, the individual connection of each electrode unit to the power supply via separate wires introduces significant difficulties in feeding a large number of electrode units, leading to increased complexity and a limited number of electrodes [27]. Moreover, the presence of multiple feeding wires causes difficulty in electrode rotation, which is required to ensure shape accuracy during wafer processing. Mohri et al. [33] proposed a high-resistivity electrode method that utilizes the distributed resistor of the electrode to achieve an equivalent division effect, thus realizing a parallel discharge. This method eliminates the need for multiple feeding wires. Specifically, the MRR achieved by a 1.5 mm-thick Si electrode with a resistivity of 0.01 Ω·cm was 2.6 times that of a copper electrode. Parallel discharge phenomena are also commonly observed in wire EDM [34], especially when utilizing an ultrafine wire electrode [35], machining workpieces with super-large thicknesses (> 1000 mm) [36], high resistance [37], or multi-wire EDM [38–40] owing to the internal resistance of the wire or workpiece, leading to improvements in the MRR. In such cases, it is necessary to consider the distributed resistor of the electrode rather than simply treating it as an electric equipotential body. However, the high resistance causes extra energy consumption and reduces the energy efficiency of EDM.

To the best of our knowledge, this is the first study to propose a capacitive electrode method for achieving high efficiency and surface quality in the flattening of large wafers. Using the electrostatic induction mechanism, the capacitive electrode readily achieved nanosecond parallel discharges without requiring individual wire connections for each electrode unit. This significantly simplifies the system configuration and improves the overall machining process performance in terms of material removal rate and surface roughness. The following section demonstrates the principle of the proposed capacitive electrode method and the fundamental mechanisms that determine the discharge behavior and

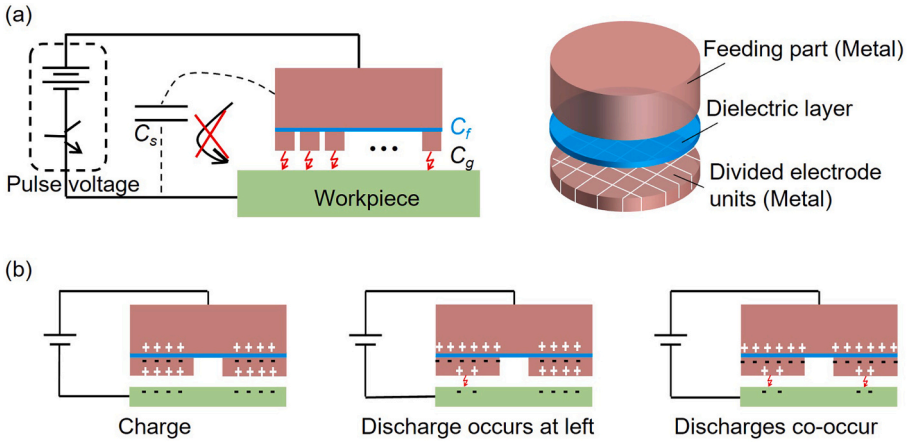


Fig. 2. Mechanism of the capacitive electrode method. (a) Schematic of the capacitive electrode method for parallel-discharge EDM; (b) Principle of parallel-discharge EDM utilizing the capacitive electrode method.

machining performance.

2. Principle of the capacitive electrode method

Controlling the discharge energy is essential for suppressing process-induced damage in the EDM of semiconductors. To overcome the difficulties of simultaneously achieving a high MRR and surface finish in large-wafer processing through EDM, the discharge frequency should be increased while maintaining a low discharge energy. In this study, we developed a novel capacitive electrode mechanism to simultaneously achieve nanosecond and massive parallel discharges using wireless feeding. The following sections detail the mechanisms of the proposed capacitive electrode method.

2.1. Generation of micro discharges by EIFM

Fig. 1 illustrates the principle of the EIFM proposed by Kunieda et al. [25]. The pulse power supply is coupled to the machining gap by feeding capacitance C_f. Upon the application of voltage, equal quantities of opposite charges accumulate in the gap between the tool electrode and workpiece through electrostatic induction, creating an electric field for discharge generation. The EIFM discharge duration, which is determined by the time constant, can be easily controlled to a few hundred nanoseconds, thus requiring no dedicated high-frequency pulse generator. Once discharge occurs, the gap voltage remains constant at a low value, that is, the discharge voltage. A new discharge does not occur until the power voltage changes substantially (e.g., falls to 0 or $-E$) in the latter half of the cycle. Therefore, the EIFM discharge interval is ensured compared with the relaxation micro-EDM method [41,42], which is beneficial for avoiding abnormal discharge or discharge concentrations. In addition, because the EIFM does not include resistor components in the circuit, it significantly reduces the capacitor charging time to achieve a higher discharge frequency and prevents losses due to Joule heating on the resistors during the EDM process. Moreover, the EIFM enables wireless or noncontact electrical feeding [43]. Leveraging these advantages, an EIFM circuit was employed in this study. However, EIFM cannot be used directly to process large wafers because of its low machining efficiency [20]. Another limitation of the EIFM is that the gap capacitance formed by large wafers limits the achievable minimum discharge energy.

2.2. Concept of capacitive electrode for massive parallel discharges

A capacitive electrode method, as depicted in Fig. 2(a), is proposed to simultaneously increase the discharge frequency by enabling massive parallel discharges and reduce the minimum discharge energy by enabling near-infinite electrode division. The electrode is capacitive because it has an internal electrostatic capacity C_f, which is realized by sandwiching a dielectric material inside the metal electrode. The internal feeding capacitance C_f of the composite electrode was serially coupled with the gap capacitance C_g to create an electrostatic induction discharge circuit [25]. The metal electrode beneath the dielectric layer is divided into multiple electrically isolated segments to reduce the large-gap capacitance. Each segment functions as an individual electrode unit, creating multiple parallel capacitively coupled discharge circuits [30].

The principle of realizing parallel discharges using the proposed method was demonstrated by employing two parallel electrode units, as illustrated in Fig. 2(b). Upon applying a power supply, both the electrode and gap capacitances are charged, with positive charges accumulating on the upper plate of the capacitance, thus developing a strong gap electric field for discharge generation. Charge transfer occurs through the discharge channel when discharge occurs in one gap (left electrode in Fig. 2b). In other words, electrons flowed from the workpiece to the left electrode unit. However, there was no charge transfer at the right electrode unit in this branch because no discharge occurred at the gap. Essentially, the charge stored in the right gap capacitance (i.e., the potential difference) remains unless a discharge occurs. This characteristic enables the simultaneous generation of parallel discharges in two- or multiple-electrode units. Thus, parallel discharge can be achieved using this capacitive electrode. The parallel discharge mechanism can increase the discharge frequency and disperse the discharge locations, thereby indicating high potential for improving the machining rate and process stability.

The unique advantage of this method is that individual feeding wires are not required to construct multiple parallel discharge circuits because power transmission from the power source to the machining gap can be realized by electrostatic induction based on this novel capacitive electrode configuration. This significantly simplifies the parallel discharge circuit system, allowing nearly infinite electrode division. By dividing the multiple electrode units, the large-gap capacitance can be decomposed into several small-gap capacitances, thereby overcoming the limitation of the minimum discharge energy imposed by the large working area. Furthermore, it inherits the advantages of the EIFM in generating ultra-short pulses and maintaining discharge stability. In addition, the capacitive electrode method causes the feeding capacitance to be closer to the discharge gap. Compared to traditional discharge circuits [44,45], the capacitive electrode method benefits minimizing the discharge energy by preventing the energy stored in the stray capacitance C_s from being released into the gap [46]. Based on the proposed technology, both small-energy microdischarges and massive parallel discharges can be simultaneously achieved, thus ensuring both process precision and efficiency for large-sized wafer fabrication. Based

Table 1
Process advantages over multi-electrode array EDM with a relaxation-type generator.

Performance	Relaxation-type generator	This method
Minium discharge energy	Larger	Smaller (no stray capacitance)
Discharge stability	Instable, uncontrolled discharge interval	Stable, ensured pulse interval
Discharge frequency	Lower due to long capacitor charging time	Higher owing to shorter capacitor charging time
Energy consumption	Energy loss due to Joule heat in resistance	No energy-consuming components
Ease of parallel discharge operation	Requires individual feeding wire →Highly complex parallel discharge circuit system	Enables wireless electrical feeding →Simplifies the parallel discharge circuit system

on the above discussions, the advantages of this method over multi-electrode array EDM with a relaxation-type generator are summarized in Table 1.

3. Equivalent circuit analysis

The quality of the machined surface is determined by the discharge energy of a single pulse. An open-gap voltage above a certain threshold value is a prerequisite for discharge generation. Both factors are influenced by the structure of the capacitive electrode, including its dielectric permittivity, thickness, and unit electrode area. Therefore, an equivalent circuit analysis that considers the design of the capacitive electrode is necessary to accurately predict the gap voltage and discharge energy. This, in turn, provides a theoretical basis for the design of capacitive electrodes.

The literature [46,47] analyzed the discharge circuit of the EIFM. However, they aimed at micro EDM, in which the stray capacitance is significantly small (<10 pF) and uncontrollable. In comparison, this study focuses on large-size wafer machining, where the gap stray capacitance during machining is significantly larger (for example, >5000 pF for 2 in wafer) compared to those in micro-EDM, hence exerting considerable influence on the discharge ignition and discharge energy. Besides, the gap stray capacitance C_g and the feeding capacitance C_f change with the electrode segmentation in the proposed multidivided capacitive electrode method. Therefore, it is necessary to perform an equivalent circuit analysis to quantitatively clarify the relationship between the key design parameters (electrode division number, dielectric layer parameter, and ratio of C_f to C_g) and the discharge characteristics in the proposed method.

3.1. Open-gap voltage for discharge breakdown

The open-state equivalent circuit with a multidivided capacitive electrode is presented in Fig. 3(a), where C_{fn} represents the internal capacitance of the capacitive electrode, C_{gn} is the gap capacitance of the machining gap, and the subscript n denotes the number of electrode units after division. Each branch corresponds to one electrode unit. For any branch, the power voltage E equals the combined voltage across the capacitive electrode V_{fn} and gap voltage V_{gn}, as expressed in Eq. (1).

$$E = V_{fn} + V_{gn} \tag{1}$$

Upon applying voltage, a charging current flows through each branch circuit to charge the capacitors. After charging, the total charge quantity Q stored in both capacitances is equal, as expressed in Eq. (2). Combining Eqs. (1) and (2), the gap voltage V_{gn} can be expressed as a function of the ratio of C_{fn} to C_{gn}, as shown in Eq. (3).

$$Q_{fn} = Q_{gn} = C_{fn}V_{fn} = C_{gn}V_{gn} \tag{2}$$

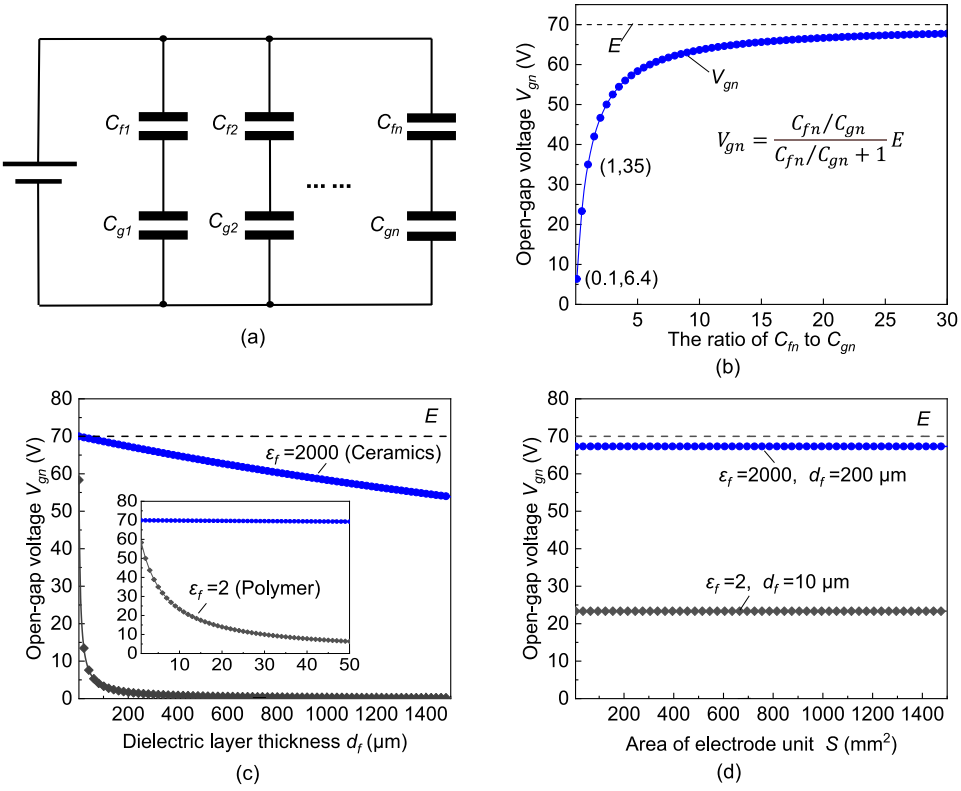


Fig. 3. Open-gap voltage obtained using the mutlidivided capacitive electrode method. (a) Equivalent circuit in open state; (b) Relationship between the open-gap voltage V_{gn} and the ratio of electrode internal capacitance to gap capacitance C_{fn}/C_{gn}; (c) Influence of the dielectric layer thickness d_f on the open-gap voltage V_{gn}; (d) Influence of the electrode unit area S on the open-gap voltage V_{gn}.

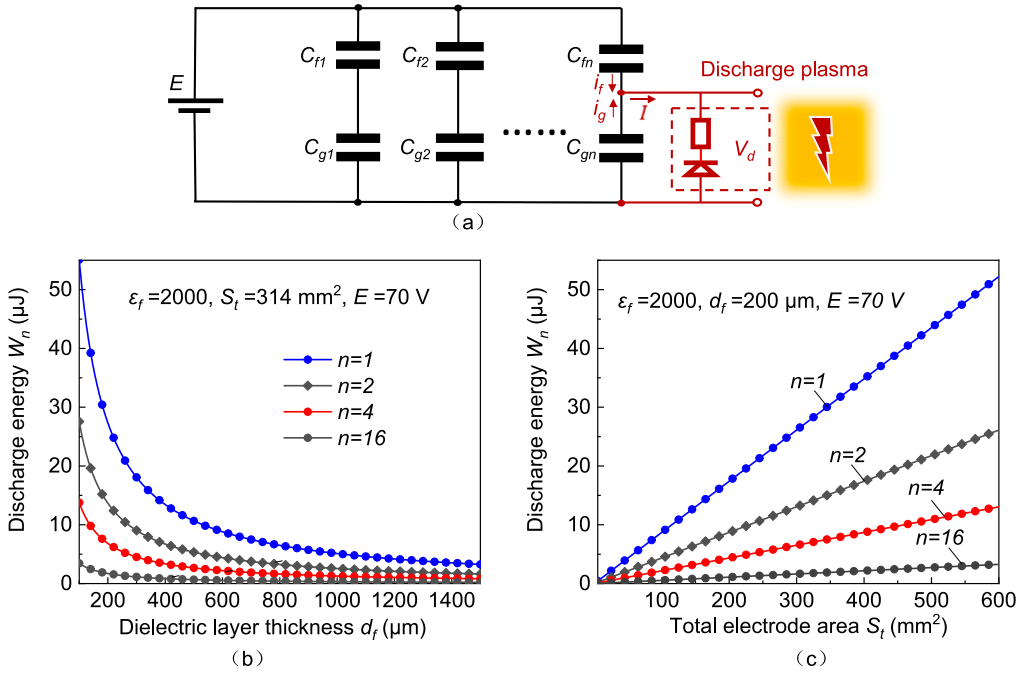


Fig. 4. Discharge energy obtained using the capacitive electrode method. (a) Equivalent circuit in discharge state; (b) Plot of discharge energy W_n over dielectric layer thickness d_f. (c) Relationship between the discharge energy and the total electrode area S_t for different n division numbers.

$$V_{gn} = \frac{C_{fn}/C_{gn}}{C_{fn}/C_{gn}+1}E \tag{3}$$

The plot in Fig. 3(b) illustrates the significant effect of the ratio of C_{fn} to C_{gn} on the open-gap voltage when power voltage E was assumed to be 70 V. A decrease in C_{fn}/C_{gn} led to a sharp reduction in the open voltage V_{gn}, accompanied by a rapid increase in the reduction rate. When C_{fn} equals C_{gn}, the open-gap voltage is attenuated by half of E. Because excessive voltage attenuation can impede discharge ignition, C_{fn} must be maintained at a magnitude comparable to C_{gn} at least. This highlights the importance of the design of the dielectric layer parameter because C_{fn} is determined by the dielectric.

By definition, the capacitance C_{fn} is expressed by Eq. (4), where ε_f and d_f represent the relative permittivity and thickness of the dielectric layer, respectively. The parameter ε_0 is the permittivity in vacuum, and S_f represents the area between each electrode unit with a dielectric layer. Similarly, C_{gn} can be expressed by Eq. (5), where ε_g is the relative permittivity of the working fluid, which typically has a value of approximately 4 for kerosene. S_g represents the area between each electrode unit and workpiece. The ratio between S_f and S_g is a constant determined by the electrode assembly method, assuming that both S_f and S_g are equivalent to the area S of each electrode unit. The parameter d_g represents the machining gap distance, which is assumed to be 10 μm to facilitate analysis.

$$C_{fn} = \frac{\varepsilon_f \varepsilon_0 S_f}{d_f} \tag{4}$$

$$C_{gn} = \frac{\varepsilon_g \varepsilon_0 S_g}{d_g} \tag{5}$$

Combining Eqs. (3)–(5), the relationship between V_{gn} and the dielectric layer parameters can be obtained as expressed in Eq. (6).

$$V_{gn} = \frac{\varepsilon_f d_g}{\varepsilon_f d_g + \varepsilon_g d_f}E \tag{6}$$

In Fig. 3(c), the influence of the dielectric layer thickness on the open-gap voltage is demonstrated considering two commonly utilized dielectric materials, namely polymer with low permittivity (ε_f=2) and ceramic with high permittivity (ε_f=2000). Increasing the thickness of the dielectric material decreases the open-gap voltage. The thickness of a polymer with a low permittivity must be reduced to a few micrometers to prevent excessive gap voltage attenuation. However, reducing the thickness increases the risk of dielectric breakdown. In other words, the discharge tends to occur through the dielectric layer instead of through the machining gap. In contrast, ceramic materials with high permittivity allow for thicker layers while satisfying the voltage requirements, thereby preventing dielectric breakdown. Therefore, it is a better material for the construction of capacitive electrodes. Furthermore, as illustrated in Fig. 3(d), once the dielectric medium and its thickness are determined, the open-gap voltage remains constant regardless of the change in the area S of each electrode unit. This enables the capacitive electrode to be divided into near-infinite units without affecting the discharge breakdown.

3.2. Single-discharge energy

The equivalent circuit of the electrode unit undergoing discharging is shown in Fig. 4(a). The equivalent circuit of the discharge channel can be described as a voltage-stabilizing diode and resistor in series. The discharge channel was connected in parallel to the gap capacitance C_{gn}. The charge transfer and charge conservation mechanisms during discharge were applied here to derive the mathematic relationship between the single discharge energy and circuit parameters. When discharging occurs, the charges pass through the discharge channel, causing charge redistribution in C_{gn} and C_{fn}. The change in charge across C_{gn} and C_{fn} before and after discharging can be expressed by Eqs. (7) and (8), respectively. The amount of charge transfer Q_C through the discharge channel equals the sum of the charge changes stored in the capacitances, as expressed in Eq. (9).

$$|\Delta Q_{gn}| = C_{gn}(V_{gn} - V_d) \tag{7}$$

$$|\Delta Q_{fn}| = -C_{fn}\left[(E - V_{gn}) - (E - V_d)\right] = C_{fn}(V_{gn} - V_d) \tag{8}$$

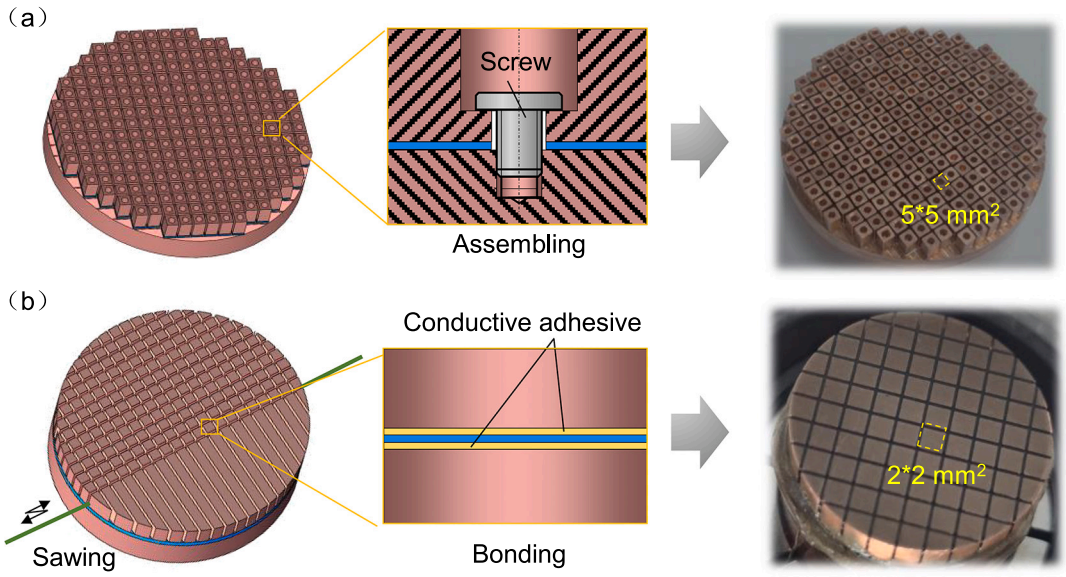


Fig. 5. Different integration methods of the sandwich-structured capacitive electrode using (a) the screw and (b) the conductive adhesive.

$$Q_c = |\Delta Q_{gn}| + |\Delta Q_{fn}| = (C_{gn} + C_{fn})(V_{gn} - V_d) \tag{9}$$

In EDM, the energy per discharge can be calculated by integrating the product of the discharge voltage V_d and current I over time. Because the discharge voltage V_d is approximately constant at 20 V in EDM, the discharge energy can be described by Eq. (10). Based on the above equations, the energy per discharge in the capacitive electrode method can be further derived and expressed in terms of the dielectric layer parameters, as shown in Eq. (11). Here, S_t indicates the total surface area of the capacitive electrode, and n indicates the number of electrode units after division.

$$W_n = \int_0^{T_e} V_d I dt = V_d Q_c \tag{10}$$

$$W_n = \frac{\varepsilon_0 S_t}{n}\left[\left(EV_d - {V_d}^2\right)\frac{\varepsilon_f}{d_f} - \frac{{V_d}^2 \varepsilon_g}{d_g}\right](n = 1, 2, 3, 4.....) \tag{11}$$

Thus, the relationship between the energy per discharge W_n, the dielectric layer thickness d_f, and the total electrode area S_t for different division numbers n can be plotted, as illustrated in Fig. 4(b) and (c). Decreasing the thickness of the dielectric layer or increasing the total electrode area led to an increase in discharge energy. As the number of subdivisions increases, the discharge energy decreases. The finer the electrode division, the lower the discharge energy. This is beneficial for achieving a high surface finish in the precision machining of large wafers.

4. Experimentation

Fig. 5 illustrates the two fabrication methods for capacitive electrodes. The use of screws allows for the convenient replacement of damaged electrode units; however, the size of the electrode unit is limited by the screw dimensions. In contrast, bonding with a conductive adhesive allows the utilization of a microwire sawing technique to divide the bottom metal plate into several very small units (for this case 2×2 mm^2). Further, the gaps among the electrodes were optimized to 200 μm to avoid discharges between the electrode units. Copper was utilized to construct the capacitive electrode because it is the preferred material for EDM of SiC in terms of promoting the MRR [48]. The dielectric layer utilized was a high-permittivity ceramic with a thickness of 0.2 mm. The division number of the capacitive electrode was varied during the experiments for comparison.

Wafer-flattening experiments employing the proposed capacitive electrode, illustrated in Fig. 6(a), were conducted to validate the proposed method. Each electrode unit within the working area was simultaneously discharged to remove material, as shown in Fig. 6(b). Specifically, an n-type 4H-SiC wafer was utilized as the workpiece, measuring an electrical resistivity of 0.015–0.028 Ω·cm. A pulse generator connected the integrated capacitive electrode and the wafer workpiece in series. The pulse generator comprises a function generator (KEYSIGHT 33600A) and a power amplifier (HSA 4101, DC ~ 10 MHz/50VA), delivering a periodical pulse voltage and current of ±71 V and 2.8 $A_{p\text{-}p}$ with a frequency ranging from DC to 10 MHz, respectively. In the experiments, a multidivided capacitive electrode was installed on

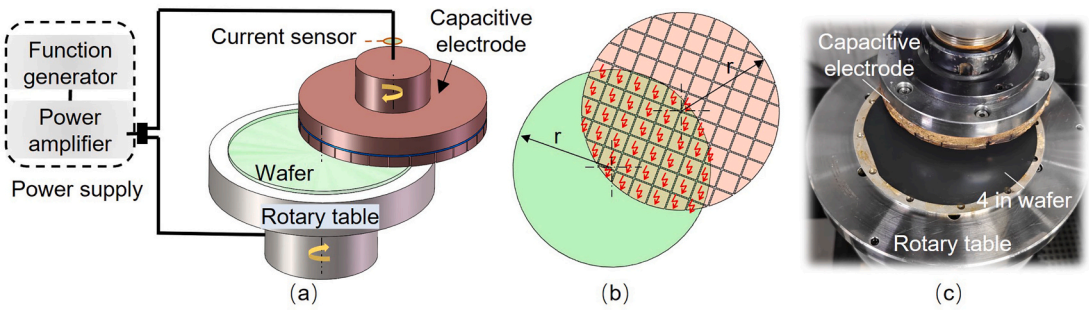


Fig. 6. Experimental setup of electrical discharge flattening using the capacitive electrode. (a) Schematic of the experimental method; (b) Insight into the working area with parallel discharges; (c) Photo of the working area of the experimental setup.

Table 2
Experimental conditions and parameters.

Parameter	Value
Pulse power supply	
Power waveform	Sinusoidal shape
$E_{p\text{-}p}$	± 70 V
Frequency f	50–200 kHz
Electrode rotation speed	50 rpm
Wafer rotation speed	20 rpm

the rotating spindle (EROWA ER-008566) of an EDM machine tool (Sodick AG40L), and the workpiece was positioned on an oil-proof, precise rotary worktable. The x-, y-, and z-axis stages of the EDM machine tool have a stepping resolution of 0.1 μm. The electrode was rotated and fed towards the counter-rotating wafer workpiece to flatten the wafer. Counter-rotating kinematics is beneficial for ensuring surface flatness and facilitating debris removal. The rotation speeds of the tool and wafer (Table 2) were determined via preliminary experiments to ensure stable and sufficient flushing of machining debris. Machining was performed using kerosene. Fig. 6(c) shows a photograph of the working area of the experimental setup. To verify parallel discharge, the current signal from the main circuit was acquired using a current sensor (Pearson 110 A) and an oscilloscope (Tektronix MDO4104C). The primary experimental conditions are listed in Table 2, unless otherwise specified.

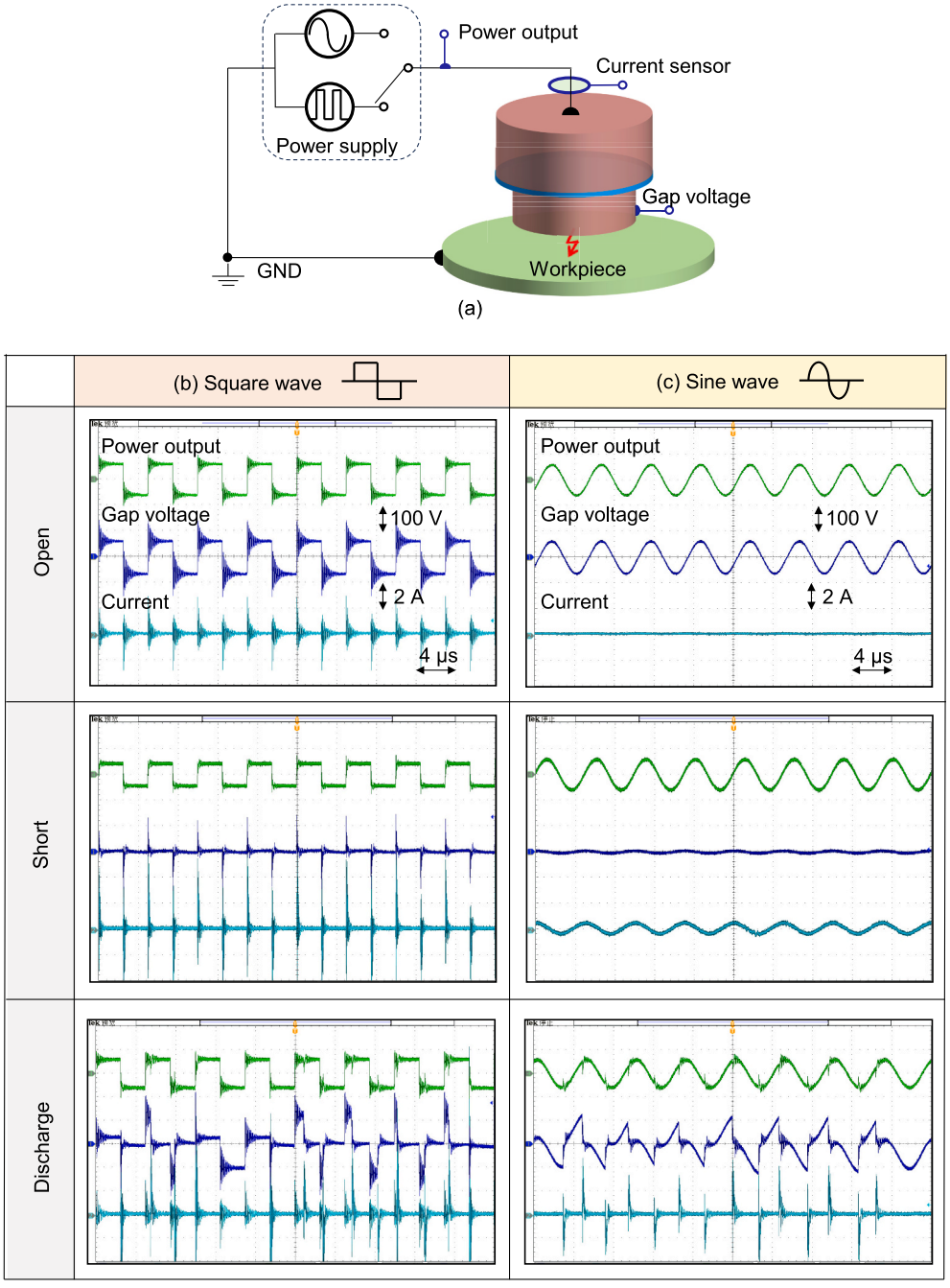


Fig. 7. Influence of the pulse voltage waveform. (a) Experiment method for measuring the gap discharge state; (b) Discharge waveform under square wave voltage; (c) Discharge waveform under sinusoidal-shape voltage.

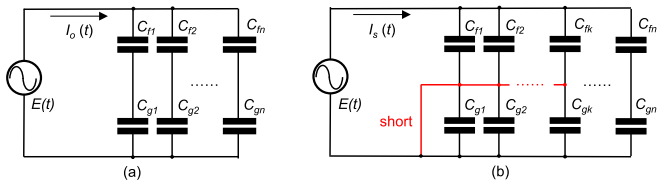
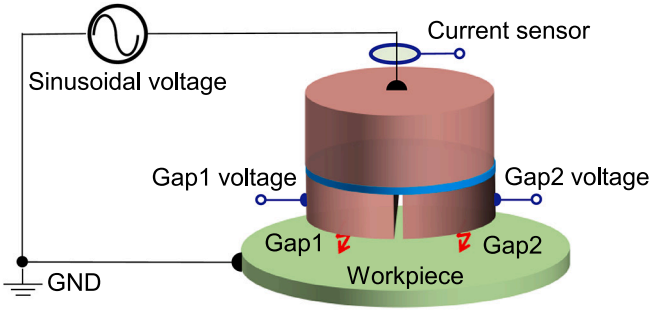


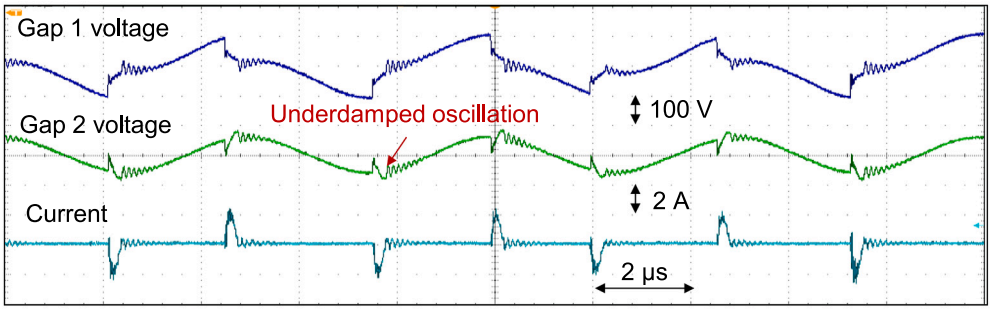
Fig. 8. Equivalent circuits of (a) open state and (b) short state.

5. Results and discussion

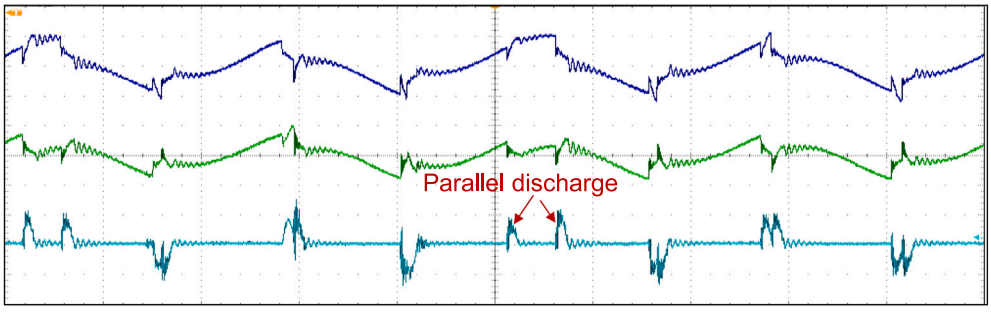
This section describes the process mechanism, machining performance, and process control method through experiments and modeling. The critical process parameters determining the parallel-discharge EDM performance, including the pulse-waveform design and capacitive electrode division method, are discussed. In particular, the superiority of the capacitive electrode method in processing large-sized 4H-SiC wafers was demonstrated through comparative studies.



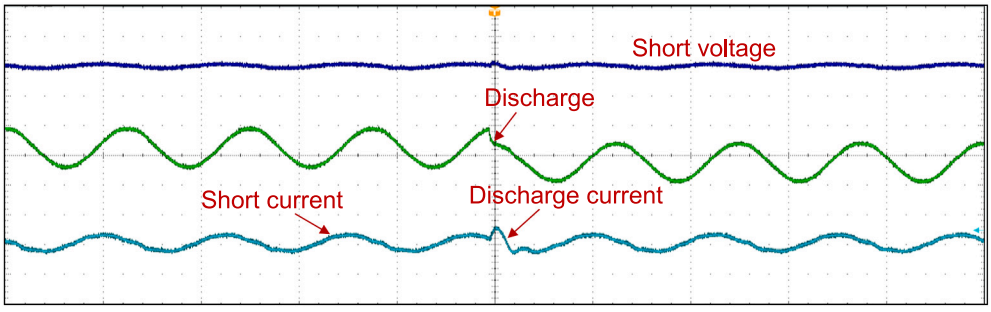
(a)



(b) Gap1 discharge & Gap2 open



(c) Gap1 discharge & Gap2 discharge



(d) Gap1 short & Gap2 discharge

Fig. 9. Verification and characteristics of parallel discharges using two electrode units. (a) Electrical signal measurement method; (b) Discharge occurring only at Gap1; (c) Discharges co-occurring at Gaps 1 and 2; (d) Discharge occurring at Gap2 and short-circuiting of Gap1.

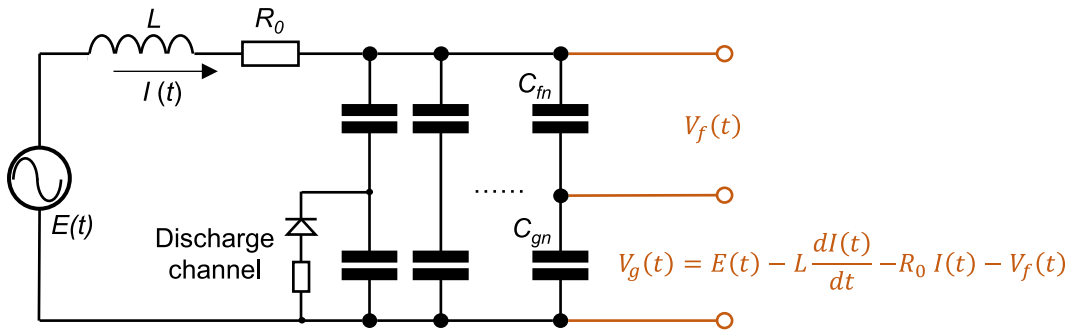


Fig. 10. Description of electrical oscillation when a discharge occurs using an equivalent circuit.

5.1. Influence of pulse voltage waveform on discharge state identification

Generally, discharge state identification in EDM relies on sampling gap voltage signals [18,49]. However, when many electrode units in a capacitive electrode are utilized for parallel discharge, detecting all the gap voltages is practically impossible, particularly on a rotating electrode. Therefore, distinguishing the discharge states from the current signal is more practical for the parallel-discharge EDM. Waveforms corresponding to different gap states under square and sinusoidal voltage supplies were investigated using a multidivided capacitive electrode with a single electrode unit of 176 mm^2. This testing method is illustrated in Fig. 7(a). The gap voltage, which is immeasurable during actual machining practice, is also presented as a reference for discriminating the discharge states. The electrode was not rotated to facilitate measurement of the gap voltage using a voltage probe (Tektronix TPP0500B).

As illustrated in Fig. 7(b), the acquired current signal waveforms of the open and short states are similar under a square-wave voltage. The displacement current flows at the rise/fall edges of the pulse because of capacitor charging, whereas the current is zero at other times. The overlap and interference between the displacement currents and normal discharge currents cause significant difficulty in recognizing a discharge event using only the current signal, particularly when the discharge delay is short. However, when a sine wave was utilized as the pulse voltage supply, the current waveforms exhibited distinct differences for different gap states, as illustrated in Fig. 7(c). The open-circuit current is close to zero, whereas the short-circuit current follows a sinusoidal waveform. The discharge current exhibited a distinct pulse shape that could be readily distinguished during discharge.

The underlying mechanism is explained by utilizing the equivalent circuit illustrated in Fig. 8, under the assumption of n electrode units. In the open state, as shown in Fig. 8(a), the circuit can be described using Eq. (12), where $I_o(t)$ represents the total current. Differentiating both sides of this equation yields the current response $I_o(t)$ of the circuit. As discussed previously, C_{fn} is much larger than C_{gn} in the circuit to minimize the voltage attenuation at the machining gap. Thus, $I_o(t)$ can be approximated using Eq. (13).

$$\int_0^T I_o(t)dt = E(t)\sum_{i=1}^{n}\frac{C_{fi}C_{gi}}{C_{fi}+C_{gi}} \tag{12}$$

$$I_o(t) = \frac{dE(t)}{dt}\sum_{i=1}^{n}\frac{C_{fi}C_{gi}}{C_{fi}+C_{gi}} \approx \frac{dE(t)}{dt}\sum_{i=1}^{n}C_{gi} \tag{13}$$

Similarly, when k electrode units cause short circuits, as illustrated in Fig. 8(b), the circuit can be described using Eq. (14), and the current response $I_s(t)$ in the short state can be expressed by Eq. (15).

$$\int_0^T I_s(t)dt = E(t)\left(\sum_{i=1}^{k}C_{fi} + \sum_{i=k}^{n}\frac{C_{fi}C_{gi}}{C_{fi}+C_{gi}}\right) \tag{14}$$

$$I_s(t) \approx \frac{dE(t)}{dt}\sum_{i=1}^{k}C_{fi} \tag{15}$$

The magnitude of the current response in the short state was significantly greater than that in the open state. This disparity arises from the significantly higher capacitance value of C_{fn} relative to C_{gn}. The current signal approached zero in the open state, whereas it displayed a sinusoidal waveform on the same scale in the short condition. The absence of voltage-step changes in the sinusoidal voltage supply prevented the generation of current pulses. Consequently, the discharge current could be accurately captured and distinguished. As the sinusoidal voltage source was proven to be more suitable for the identification of parallel discharge conditions, it was selected as the voltage supply for subsequent experiments.

5.2. Parallel discharge characteristics

The discharge characteristics of the multidivided capacitive electrode were investigated by analyzing the discharge voltage and current waveforms. A simplified capacitive electrode with two electrode units of 157 mm^2 was employed to study the fundamental parallel discharge behavior. As illustrated in Fig. 9(a), the gaps between the two electrode units and the workpiece were designated as Gap1 and Gap2, and their gap voltages, V_{g1} and V_{g2}, were measured using two voltage probes. The total current in the main circuit was measured using a current sensor. A sinusoidal voltage source was applied to facilitate the identification of parallel discharge states.

The measurement results for different gap conditions are shown in Fig. 9(b), (c), and (d). As shown in Fig. 9(b), when the discharge ignites at Gap1, the charges stored in the gap capacitance begin to flow, causing a rapid decrease in the gap voltage. The discharge duration is extremely short, lasting only 400 ns, owing to the direct discharge through the capacitors. Meanwhile, Gap2 in the open state undergoes a momentary voltage drop of approximately 50 V, followed by a subsequent rise and an underdamped oscillation. The overall voltage waveform is aligned with the sinusoidal waveform of the power supply. Notably, there are instances when the voltage momentarily exceeds the original gap voltage by approximately 10–20 V, owing to voltage oscillation. This phenomenon plays a beneficial role in promoting discharge in other electrode gaps. As illustrated in Fig. 9(c), when Gap1 was discharged, it was immediately followed by discharge at Gap2. The voltage oscillation after discharge is attributed to the induced electromotive force generated by the distributed inductance in the electric feeding wires. The equivalent circuit in Fig. 10 explains the circuit oscillation, where L represents the inductance, and R_0 is the resistance in the main circuit. According to Kirchhoff's voltage law (KVL), the oscillation behavior in terms of the gap voltage can be described using Eq. (16).

$$L\frac{dI(t)}{dt} + R_0 I(t) + V_g(t) + V_f(t) = E(t) \tag{16}$$

Because the inductance stores and releases energy during the

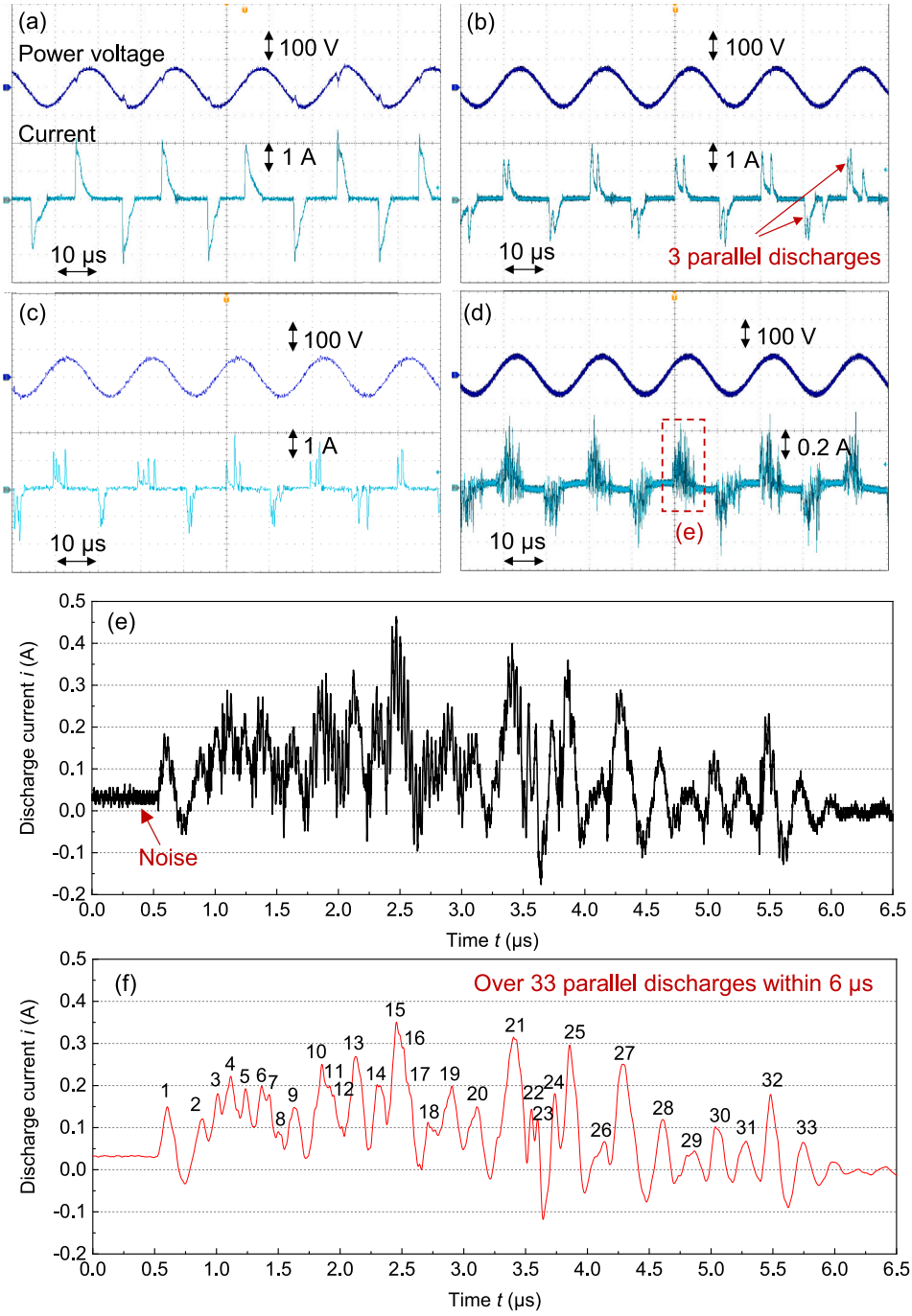


Fig. 11. Discharge waveforms of the capacitive electrode with various division numbers: (a) without division; (b) divided into 2 units; (c) divided into 4 units; (d) divided into 88 units. (e) Enlarged view of parallel-discharge currents in a single pulse; (f) The current waveform of (e) after filtering the noise using the moving average method. Over 33 parallel discharges with pulse widths below 200 ns within 6 μs in a single pulse is observed.

discharge process, as the discharge current changes, the current does not immediately decrease to zero when the discharge ends. Instead, it induces oscillations in the current and voltage. In addition, resistance in the circuit causes energy loss, leading to underdamped oscillation behavior.

Furthermore, when Gap1 was short-circuited, the voltage at Gap2 remained unaffected. The discharge in Gap2 can still occur independently, as shown in Fig. 9(d). In this case, the short-circuiting current of Gap1 overlapped with the discharge current of Gap2 in the measured current waveform. These observations indicate that the electrical potential of the parallel machining gaps is independent and remains unaffected by other gap conditions (discharge or short-circuiting). This provides the necessary conditions for a parallel discharge.

5.3. *Discharge frequency and single-discharge energy with the division of electrode*

The discharge waveforms of the multidivided capacitive electrode with a diameter of 20 mm under the four different scenarios are presented in Fig. 11. As the number of electrode units increases, more parallel discharge current pulses are observed under the same power supply conditions. However, when the number of electrode units was very large, the observed number of parallel discharges was smaller than that of the electrode units. This can be attributed to a decrease in the

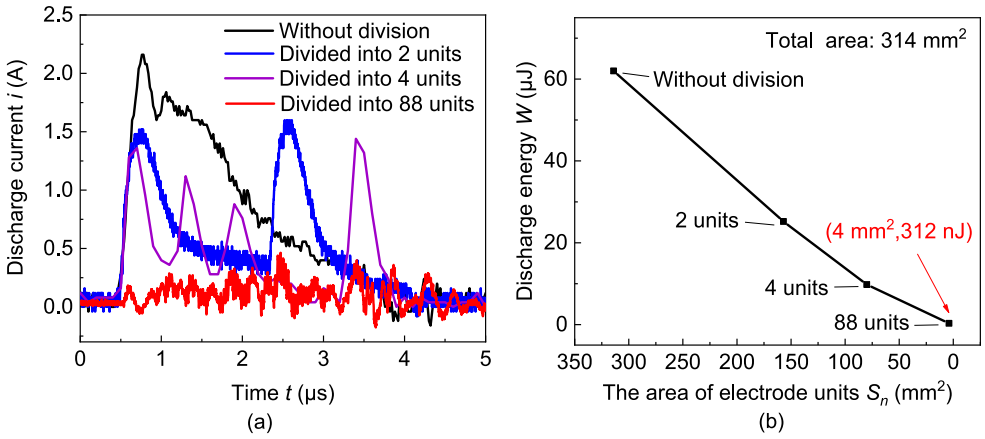


Fig. 12. Comparison of the single-discharge energy. (a) Discharge current waveform with different electrode units; (b) Variation of discharge energy with the unit electrode area.

probability of discharge with a reduction in the surface area of the unit electrode. Nevertheless, as shown in Fig. 11(d-f), over 33 parallel discharges with a pulse width below 200 ns can be obtained within 6 μs throughout a single pulse utilizing the capacitive electrode with 88 divisions, which represents a >30-fold increase in discharge frequency. From the experimental results, the parallel discharge rate, i.e., the actual discharge number in a single pulse relative to the electrode division number (for the case of 88 divided electrode), was approximately 40 %.

Furthermore, according to the waveform of the discharge state in Fig. 7, the gap voltage exhibits a significant difference between the sinusoidal and square voltage supplies when discharge occurs. The gap voltage after discharge remained constant at a low value (commonly known as the discharge voltage of 20 V [18]) under a square-voltage supply. In contrast, when a sinusoidal power voltage supply is applied, the gap voltage continues to increase along the sinusoidal curve despite the occurrence of discharge, especially when the first discharge occurs before the voltage reaches a sinusoidal peak. That is, after discharging, the gap capacitance is recharged as the power voltage increases with a sinusoidal wave, and there is a certain probability of another discharge occurring in the same unit. As illustrated in Fig. 11(b), three parallel discharges are observed when there are only two electrode units, indicating that a sinusoidal voltage supply can enhance the discharge

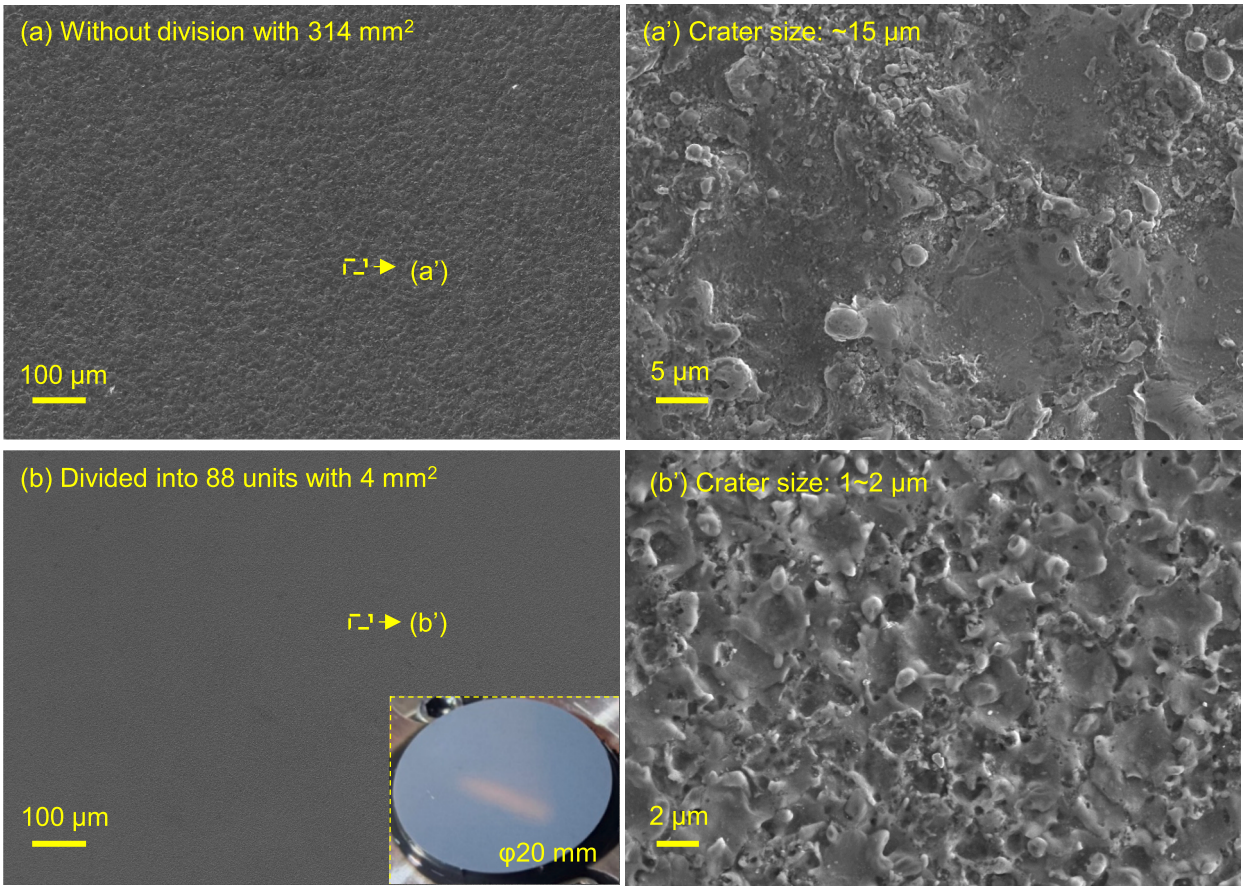


Fig. 13. Comparison of surface microtopography machined by electrode unit areas of (a) 314 mm^2 and (b) 4 mm^2 and the corresponding discharge crater sizes of (a') 15 μm and (b') 1–2 μm, achieving the optimal Ra = 42 nm surface finish on SiC through EDM.

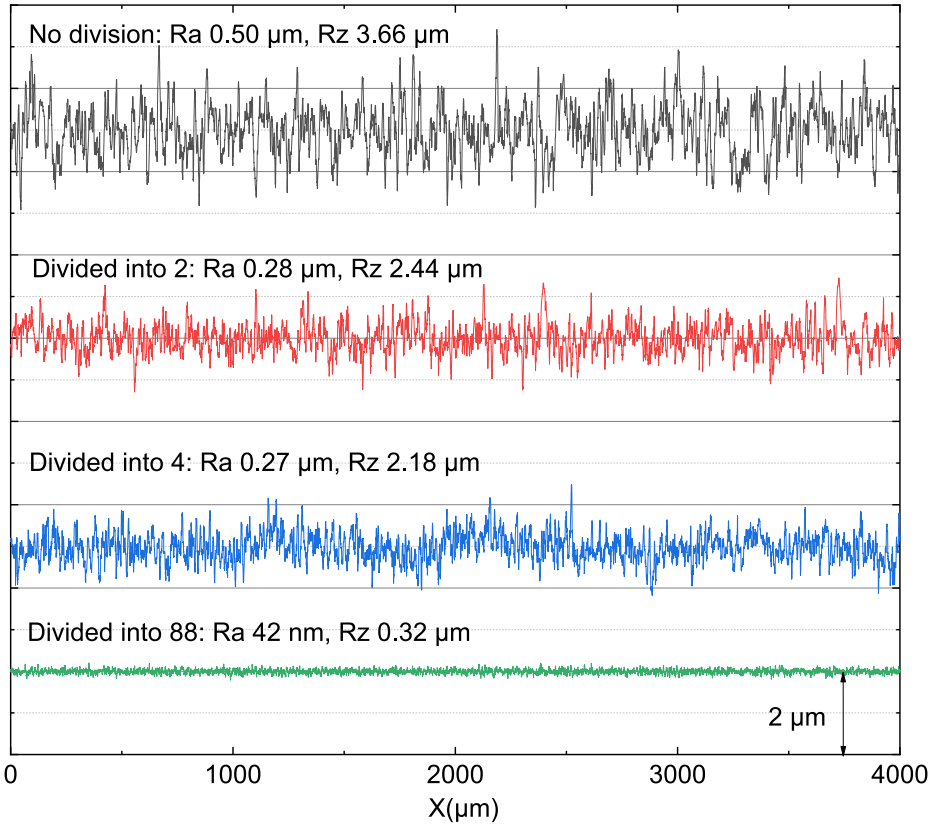


Fig. 14. Surface roughness of the wafer surface processed using the capacitive electrode method. A cone-shaped stylus with a 2 μm tip radius is utilized for measurement.

frequency through this mechanism.

However, discrepancies in the discharge energies among parallel discharges were observed, particularly when several parallel discharges occurred. The current peaks of the parallel discharges exhibited a profile resembling a sine wave, with higher values in the middle and lower values at the sides. This could be attributed to two factors. First, the discharge energy was positively correlated with the discharge voltage, as expressed in Eq. (11). Second, higher voltages increase the likelihood of discharge. Consequently, a pronounced current peak can result from the simultaneous superposition of multiple small-energy discharges.

A comparative analysis of the individual discharge current waveforms obtained under different electrode divisions is illustrated in Fig. 12(a). The duration and peak value of the discharge current decreased significantly as the number of electrode divisions (i.e., electrode units) increased, resulting in reduced discharge energy. Based on the first current pulse illustrated in Fig. 12(a), the variation in single-discharge energy with changes in the electrode unit area is plotted in Fig. 12(b). The results demonstrate that the discharge energy is linearly related to the electrode area. Compared to the electrode with no division, the energy of a single discharge is reduced by two orders of magnitude by dividing the electrode into 88 units of 4 mm^2, decreasing from 62 to 0.312 μJ. The peak value of the corresponding current is 0.18 A, with a duration of approximately 160 ns. The underlying mechanism is that electrode segmentation reduces the area and, consequently, the capacitances of C_{fn} and C_{gn}, thereby reducing the discharge energy (see Eq. (11)).

5.4. Surface finish with multidivided capacitive electrode

The topography of the machined surface as viewed using scanning electron microscopy (SEM; Zeiss Merlin) is shown in Fig. 13. The discharge crater size decreased with an increase in the number of electrode units, validating the reduced energy of a single discharge. The finest machined surface exhibited a discharge crater diameter of 1–2 μm. The roughness of the machined surface was measured using a stylus (SURFCOM NEX 031), as shown in Fig. 14. Finer electrode segmentation results in lower surface roughness. A surface with Ra = 42 nm was obtained when the electrode was divided into 88 units of 4 mm^2. Compared to the minimum surface roughness Ra = 120 nm achieved in a φ20 mm SiC using Relaxation-type generator [15], the proposed method provides a 65 % reduction in surface roughness. This shows the superiority of the capacitive electrode method for very low-damage and high-precision surface finishing applications.

5.5. Machining demonstration on a large-size wafer of 4 in

While the single-discharge energy is kept constant at a very low value (for finishing purposes), the total MRR can be improved using a multi-divided capacitive electrode by increasing the discharge frequency via a parallel discharge mechanism. As illustrated in Fig. 15(a), comparative experiments were conducted on 4H-SiC wafers with diameters of 20, 50 (2 in), and 100 mm (4 in). In the experiments, the tool electrode diameter was maintained to be consistent with that of the workpiece wafer. The unit electrode area was maintained at approximately 157 mm^2 to obtain the same single-discharge energy, according to Eq. (11). The corresponding discharge waveforms are depicted in Fig. 15(b) and (c), which demonstrate that the single-discharge energies are similar, and the number of parallel discharges increases significantly when processing 4 in wafers because a larger working area allows more electrode units to work in the gap. Under a sinusoidal power supply with an amplitude of 70 V and a frequency of 50 kHz, the achieved maximum feeding speeds are 1.3, 2.4, 1.3, and 0.5 μm/min from Cases 1 to 4 (Fig. 15a), respectively. From Fig. 15(d), for a 50 μm machining depth, which was conducted three times to ensure consistency, the MRR in

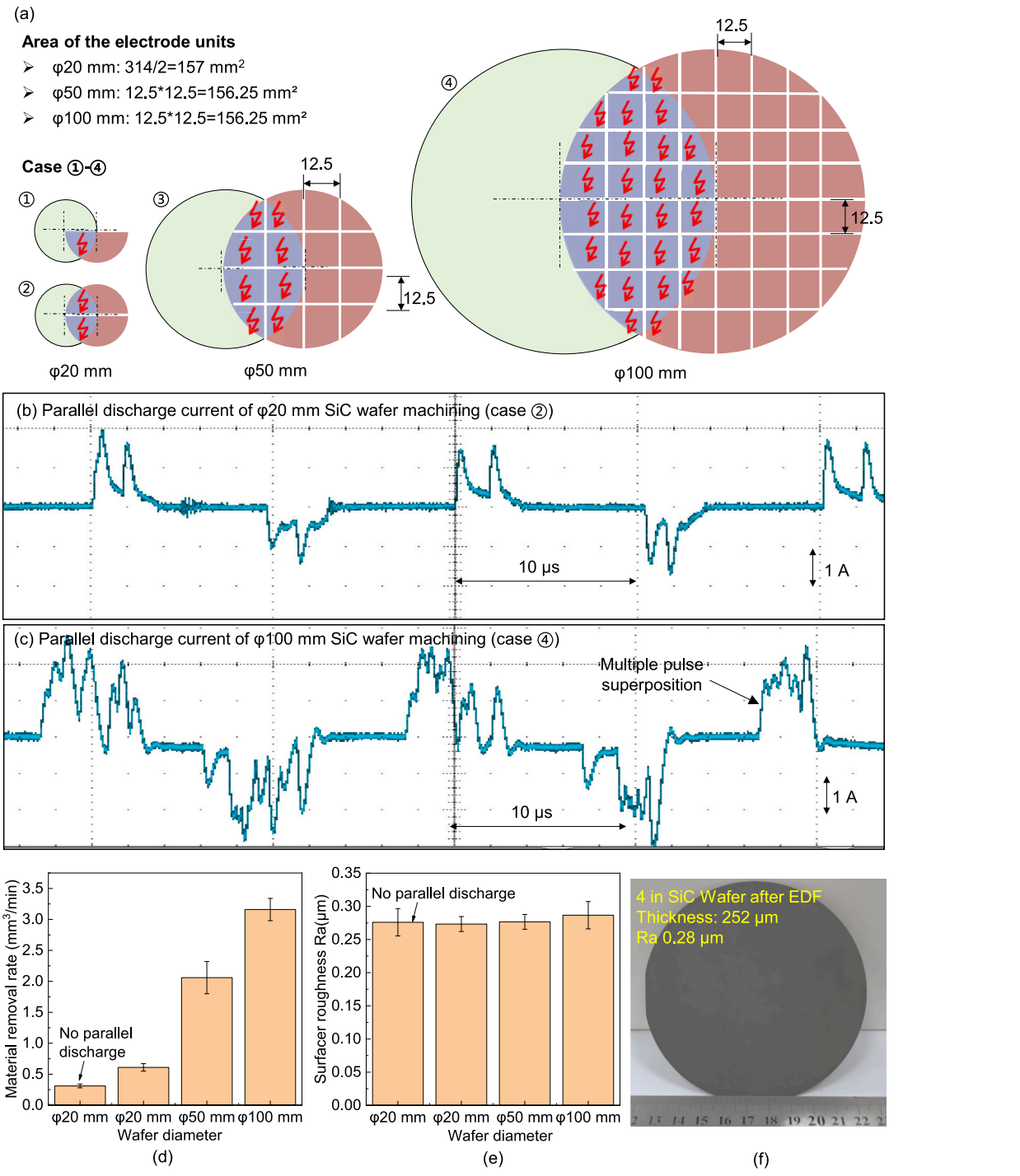


Fig. 15. Parallel discharge linearly improves the machining efficiency while maintaining the achievable surface roughness. (a) Schematic of the relationship between electrodes, electrode units, and wafer size; parallel discharge waveforms with wafer sizes of (b) φ20 mm and (c) φ100 mm; (d) increase in volumetric MRR; (e) maintained surface roughness regardless of wafer size; (f) machined sample of 4 in 4H-SiC wafer.

volume for the φ100 mm (4 in) wafer is 1.5 times higher than that of the φ50 mm (2 in), nearly 10 times higher than that of the φ20 mm with no parallel discharge condition. In addition, owing to the similar single-discharge energies, the surface roughness achieved was nearly the same, as illustrated in Fig. 15(e). Here, the surface roughness measurements were performed three times for each experiment. The variations in the surface roughness arising from systematic or random errors in the experimental process are represented by the standard deviation (SD) of the measured data. A machined sample of the 4 in wafer is shown in Fig. 15(f). Notably, the experimental results verify that the capacitive electrode method can maintain a very low surface roughness irrespective of the increase in wafer size. This was attributed to the mechanism by which the surface roughness was determined only by the unit electrode area. Moreover, the volumetric MRR can be significantly improved because the number of electrode units increases proportionally with the wafer size. This is particularly advantageous for machining large wafers.

In terms of energy consumption, the capacitive electrode parallel discharge method has no energy-consuming resistance in the circuit. Assuming the same energy of single discharge, the energy consumption

of the parallel discharge method is approximately the same as that without parallel discharges for the same material removal. However, since the parallel discharge method can significantly reduce the machining time, as revealed in Fig. 15(d), the energy consumption of the peripheral equipment such as pump, XY table, CNC and so on will be reduced.

6. Conclusion

A multidivided capacitive electrode-based parallel EDM method for the precision flattening of large-sized SiC wafers was demonstrated. This novel method minimizes the discharge energy and simultaneously maximizes the number of parallel discharges, thus ensuring both high machining efficiency and a good surface finish in large-wafer flattening. The key conclusions are as follows:

(1) The capacitive electrode method allows near-infinite division of the electrode because the power supply is wirelessly coupled to the discharge gap via electrostatic induction. Increasing the electrode division number reduces the unit electrode capacitance and gap capacitance, thereby minimizing the discharge energy. This is beneficial for improving the surface smoothness and residual stress of large-area wafers. A model describing the correlation between the electrode capacitance and discharge ignition/energy was used to explain the parallel discharge behavior and was validated through experiments. Using the capacitive electrode method, the best surface roughness Ra of 42 nm on 4H-SiC via EDM was achieved with an electrode unit area of 4 mm^2. >33 parallel nanosecond discharges (< 200 ns) within 6 μs in a single pulse are demonstrated for the first time.
(2) The identification of the overall discharge state relies on the discharge current signal. A sinusoidal voltage source produces more distinct current signals in the open, short-circuit, and discharge states than square voltage pulses. When a sinusoidal voltage was applied, the gap voltage maintained a sinusoidal change despite the occurrence of discharge. Therefore, multiple discharges were possible within the same pulse for the same electrode unit. This makes the sinusoidal voltage input superior to the conventional square pulse voltage in promoting more parallel discharges.
(3) With the capacitive electrode method, given the same unit electrode area, the volumetric MRR improved proportionally with the wafer size by increasing the electrode unit number. Meanwhile, a very low surface roughness can be maintained regardless of the increase in wafer size because the discharge energy is determined by the unit electrode area. Owing to this advantage, the capacitive electrode method has immense potential for ensuring both process efficiency and surface quality, particularly for large wafer fabrication.

CRediT authorship contribution statement

Junming Guan: Writing – original draft, Visualization, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Hongqiang Wang:** Visualization, Methodology, Formal analysis. **Masanori Kunieda:** Visualization, Investigation, Formal analysis. **Yonghua Zhao:** Writing – review & editing, Writing – original draft, Visualization, Supervision, Project administration, Methodology, Investigation, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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